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INTRODUCTION TO CMOS CIRCUITS CONTENTS

1: Circuits & Layout CMOS VLSI Design Slide 6 Transistor Types qBipolar transistors " npn or pnp silicon structure " Small current into very thin base layer controls large currents between emitter and collector " Base currents limit integration density qMetal Oxide Semiconductor Field Effect Transistors " nMOS and pMOS MOSFETS

Lecture 1: Circuits & Layout - Harvey Mudd College

CMOS Technology

- Properties of microelectronic materials
- resistance, capacitance, doping of semiconductors
- Physical structure of CMOS devices and circuits
- pMOS and nMOS devices in a CMOS process
- n-well CMOS process, device isolation
- Fabrication processes
- Physical design (layout)

Review: CMOS Logic Gates - Michigan State University

In this section, we sequentially address the design of various static circuit flavors including complementary CMOS, ratioed logic (pseudo-NMOS and DCVSL), and pass-transistor logic. The issues of scaling to lower power supply voltages and threshold voltages will also be dealt with.

6.2.1 Complementary CMOS

A static CMOS gate is a combination of two networks, called the pull-up network (PUN) and the pull-down network (PDN) (Figure 6.2).

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